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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,931	03/28/2007	Ronald Ribeiro Duarte	033794/311439	9145

826 7590 11/12/2009

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EXAMINER	
BHAT, ADITYA S	
ART UNIT	PAPER NUMBER
2863	

MAIL DATE	DELIVERY MODE
11/12/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/595,931	RIBEIRO DUARTE, RONALD	
	Examiner	Art Unit	
	ADITYA BHAT	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 14-25* is/are rejected.

7)☒ Claim(s) *12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status

1. Claims 1-25 are currently pending in this application.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. The objection to the disclosure have been withdrawn in view of applicants amendments.

Information Disclosure Statement

4. No information disclosure statement (IDS) has been submitted with the response dated 7/20/2009.

Drawings

5. The drawings submitted on 5/19/2006 are in compliance with 37 CFR § 1.81 and 37 CFR § 1.83 and have been accepted by the examiner.

Claim Objections

6. Objections to claims 1-25 have been withdrawn in view of applicant's amendments

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 23-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Khudoshin (USPN 5,734,289).

With regards to claim 23, Khudoshin (USPN 5,734,289) teaches a method of controlling the triggering of a TRIAC (TR), the TRIAC comprising a gate (G) and being electrically connected to a network voltage (V.sub.AC), the TRIAC (TR) being selectively actuated upon a pulse at the gate (G) to apply the network voltage (V.sub.AC) to a load, enabling the circulation of a current (i.sub.c), the method comprising the steps of:

applying a pulse at the gate when the current value reaches a minimum value, establishing a voltage limit value (+limit, -limit) at the gate (G) to generate the pulse at the gate (G) of the TRIAC (TR) for keeping it in conduction, the pulse at the gate (G) being generated in a previously established measurement time (t.sub.M), the measurement time (t.sub.M) occurring before the passage of the level of the current by zero, (figure 1)

measuring the current that circulates in the load,(Col. 1, lines 40-44) The controller must measure the current in order to know what it is controlling. and

adjusting the level of the voltage limit value (+limit, -limit) at the gate (G) by a control unit (12) in a proportional way to level of the current (Col.2,lines 61-67)

With regards to claim 24, Khudoshin (USPN 5,734,289) teaches the current is continuously measured. (col.1, Lines 40-45)

With regards to claim 25, Khudoshin (USPN 5,734,289) teaches the step of applying the pulse at the gate (G) of the TRIAC regulating the level of voltage in the load from the delay in generating the pulses at the gate(11;figure 1)

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-3,6-11, 14-18 and 20-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Khudoshin (USPN 5,734,289).

With regards to claim 1, Khudoshin (USPN 5,734,289) teaches a system of controlling and triggering a TRIAC (TR), the TRIAC comprising a gate (G), the TRIAC (TR) being connected to a load, the gate (G) being electrically connected to a power unit (3) that actuates the TRIAC (TR) for selectively applying a network voltage to the load and enabling the circulation of an electric current in the load, the system comprising:

a detection unit for detecting gate voltage; (Col. 2, lines 62-63)

a detection unit for detecting the passage of the feed network voltage by zero; (10;figure 1)

a power unit (1;figure 1); and

a control unit (12;figure 1);

the voltage detection unit (6,10) being electrically connected to the control unit (12) (figure 1),

the control unit establishing a gate (G) voltage limit value (+limit, -limit), and generating a pulse at the gate (G) of the TRIAC (TR) to keep it in conduction, (11;figure 1)

the pulse at the gate (G) being generated from a comparison between the voltage limit value (+limit, -limit) established by the control unit and a voltage measured at the gate (G) from the gate voltage detection unit. (Col. 2, lines 63-67)

Khudoshin (USPN 5,734,289) discloses the claimed invention except for an adjustable gate .It would have been obvious to one having ordinary skill in the art at the time the invention was made to include an adjustable gate, since it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 (CCPA 1954).

With regards to claims 2 and 18, Khudoshin (USPN 5,734,289) teaches the control unit measures the electric current and adjusts the voltage limit value (+limit, -limit) in a proportional way to the current value measured. (Col. 3, Lines 35-42)

With regards to claims 3 and 22, Khudoshin (USPN 5,734,289) teaches the control unit (4) generates the pulse at the gate (G) of the TRIAC (TR) in previously established a measurement time (t.sub.M), the measurement time occurring before the passage of the current by zero. (Col. 3, Lines 30-44)

With regards to claims 6 and 20, Khudoshin (USPN 5,734,289) teaches the adjustment of the limit (+limit, -limit) is made by means of a table of preestablished values stored in the control unit. (9;fig 1)

It is well known in the art that logic gates such as the AND gate in figure one have predetermined outputs based on the inputs. (col.3, lines 11-17)

With regards to claim 7, Khudoshin (USPN 5,734,289) teaches the detection unit (1) for detecting voltage at the gate (G) comprises a comparator electrically connected to the gate (G) of the TRIAC (TR) and to a digital-to-analog (D/A) converter, the comparator receiving the signal of the voltage at the gate (G) of the TRIAC (TR) and a signal generated by the D/A converter, the D/A converter receiving a digital signal generated by the control central (44), the signal generated by the control central (44) establishing an adjustment voltage value, the adjustment voltage value being equal to the limit values. (figure 1)

As it is well known in the art a triac is a analog component and a AND gate is a digital component. Thus the input to the pulse generator (AND output) is therefore a digital input and the output (4) of the pulse generator must be a analog (input to triac).

With regards to claim 8, Khudoshin (USPN 5,734,289) teaches a power unit, the power unit being associated to the control unit and generating a voltage pulse at the gate of the TRIAC (TR) upon a command from the control central. (figure 1)

With regards to claim 9, Khudoshin (USPN 5,734,289) teaches the control unit (4) comprises a digital-to-analog (D/A) converter, the digital-to-analog converter generating the adjustment voltage value. (11;figure 1)

With regards to claim 10, Khudoshin (USPN 5,734,289) teaches the pulse at the TRIAC (TR) is generated when the control central (44) detects a transition of level of the comparator output. (figure1)

With regards to claim 11, Khudoshin (USPN 5,734,289) teaches the control central (44) commands the digital-to-analog (D/A) converter to commute between a positive voltage limit (+limit) to a negative limit (-limit) and vice-versa at every transition received by the comparator.

With regards to claim 14, Khudoshin (USPN 5,734,289) teaches the digital-to-analog (D/A) converter is internal with respect to the control central. (figure 1) see claim 7 rejection.

With regards to claim 15, Khudoshin (USPN 5,734,289) teaches the comparator (7,8) is internal with respect to the control central. (figure 1)

With regards to claim 16, Khudoshin (USPN 5,734,289) teaches the power control unit is an internal switch of the control central (figure 1).

With regards to claim 17, Khudoshin (USPN 5,734,289) teaches method of controlling the triggering of a TRIAC (TR), the TRIAC comprising a gate (G) and being electrically connected to a network voltage (V.sub.AC), the TRIAC (TR) being selectively actuated upon a pulse at the gate (G) to apply the network voltage (V.sub.AC) to a load, enabling the circulation of a current (ic), a comparator being associated to the gate (G) of the TRIAC (TR), the method comprising:

applying a pulse at the gate (G) when the voltage limit value (+limit, -limit) at the gate (G) has been detected, the pulse being generated: from a transition at the

comparator (CP.sub.1), the comparator comparing the voltage limit voltage (+limit, -limit) at the gate (G) and a voltage measured at the gate (G), (11;figure 1)

commuting an input of the comparator from the positive voltage limit (+limit) and to a negative limit (-limit) and vice-versa at every transition received by the comparator.(col. 2, lines 63-67)

Khudoshin (USPN 5,734,289) discloses the claimed invention except for using a single comparator. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use one comparator instead of two as the comparison process would be functionally equivalent whether using one comparator or two. Further it would be highly desirable for one of ordinary skill in the art to use fewer components as this would cut production costs.

With regards to claim 21, Khudoshin (USPN 5,734,289) teaches the voltage pulse at the gate has duration sufficient for the current circulating in the TRIAC (TR) to reach a latch value. (11;figure 1)

11. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khudoshin (USPN 5,734,289) in view of Liu (USPN 5,994,883).

With regards to claim 4, Khudoshin (USPN 5,734,289) does not appear to explicitly teach a current sensor.

Liu (USPN 5,994,883) teaches the control unit obtains the current value from a current sensor. (32; Col. 3, Lines 33-36)

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the Khudoshin (USPN 5,734,289) reference to include the current

sensor taught by Liu (USPN 5,994,883) in order to arrive at the claimed invention as it would be desirable to monitor the current in order to help protect the control circuit and load from over current. (col.2, Lines 10-11)

12. Claims 5 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khudoshin (USPN 5,734,289)

With regards to claims 5 and 19, Khudoshin (USPN 5,734,289) teaches the adjustment of the limit value (+limit, -limit) is made by means of the equation: Kxl_c wherein k is a previously determined proportionality constant.

While the prior art of record does not teach the specific claimed equation. It does teach adjusting the voltage (Col.2-3, lines 60-67 &1-15) based on the threshold/limit value. As the functionality of both the prior art and the claimed invention are the same and the operating characteristics of the circuitry shown in the prior art could be interpreted as an equation by one of ordinary skill in the art at the time of the invention. It would appear that the claimed limitations would be would be an obvious modification of the prior art as the claimed equation is absent any criticality.

Allowable Subject Matter

13. Claims12-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Should applicant choose to add the limitations of claims 12-13 into claim 1 applicant is urged to point out exactly what is novel about the claimed circuit arrangement. Since the individual components i.e. resistive divider, comparator etc are

well known elements in the art, applicant should describe what exactly about this configuration makes the claimed invention patentable over the prior art.

Response to Arguments

14. Applicant's arguments with respect to claims1-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

16. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ADITYA S. BHAT whose telephone number is (571)272-2270. The examiner can normally be reached on M-F 9-5:30.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Dunn can be reached on 571-272-2312. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aditya Bhat/
Primary Examiner, Art Unit 2863
November 9, 2009